

COPY OF PAPERS
ORIGINALLY FILED

Attorney Docket No.: 00CON159P-C1



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

Hassan S. Hashemi

Serial No.: 09/713,834

Filed: November 15, 2000

For: **Leadless Chip Carrier Design
And Structure**

Art Unit: 2827

Examiner: Lourdes C. Cruz

RECEIVED
JUN 28 2002
TECHNOLOGY CENTER 2800

#15/2
7/22/2
Lmth
Ex

AMENDMENT AND RESPONSE TO OFFICE ACTION

Honorable Commissioner of
Patents and Trademarks
Washington, D.C. 20231

Dear Sir/Madam:

This is in response to the Office Action dated March 4, 2002 in the above-referenced patent application. Please enter and consider the following amendments and remarks.

06/25/2002 SSESHE1 00000111 09713834

01 FC:115

110.00 OP

In the Claims:

Marked up version of once amended claim 18:

18. (Once Amended) A structure comprising:
a substrate having a top surface for receiving a chip;
a printed circuit board attached to a bottom surface of said substrate;
at least one signal via in said substrate;
said at least one signal via providing an electrical connection between a device
electrode of said chip and said printed circuit board;
a plurality of separate thermally conductive vias in said substrate, each of said
plurality of separate thermally conductive vias being coupled to a heat spreader, said heat
spreader being attached to said bottom surface of said substrate.

Clean version of once amended claim 18:

18. A structure comprising:
a substrate having a top surface for receiving a chip;
a printed circuit board attached to a bottom surface of said substrate;
at least one signal via in said substrate;
said at least one signal via providing an electrical connection between a device
electrode of said chip and said printed circuit board;

B1
a plurality of separate thermally conductive vias in said substrate, each of said plurality of separate thermally conductive vias being coupled to a heat spreader, said heat spreader being attached to said bottom surface of said substrate.

Marked up version of once amended claim 23:

23. (Once Amended) The structure of claim 18 wherein said at least one signal via provides an electrical connection between a bond pad and said printed circuit board, wherein said bond pad is electrically connected to said device electrode.

Clean version of once amended claim 23:

B2
23. The structure of claim 18 wherein said at least one signal via provides an electrical connection between a bond pad and said printed circuit board, wherein said bond pad is electrically connected to said device electrode.

Marked up version of once amended claim 24:

24. (Once Amended) The structure of claim 23 wherein said at least one signal via abuts said bond pad.

Clean version of once amended claim 24:

24. The structure of claim 23 wherein said at least one signal via abuts said bond pad.

Marked up version of once amended claim 26:

26. (Once Amended) The structure of claim 18 wherein said at least one signal via provides an electrical connection between said device electrode and a land, said land being electrically connected to said printed circuit board. ¹⁰⁴ (from 14A)

Clean version of once amended claim 26:

26. The structure of claim 18 wherein said at least one signal via provides an electrical connection between said device electrode and a land, said land being electrically connected to said printed circuit board.

B3 **Marked up version of once amended claim 27:**

27. (Once Amended) The structure of claim 26 wherein said at least one signal via abuts said land.

Clean version of once amended claim 27:

27. The structure of claim 26 wherein said at least one signal via abuts said land.

Marked up version of once amended claim 28:

28. (Once Amended) The structure of claim 18 wherein said at least one signal via provides an electrical connection between a bond pad and a land, wherein said bond pad is electrically connected to said device electrode, and wherein said land is electrically connected to said printed circuit board.

Clean version of once amended claim 28:

B3
28. The structure of claim 18 wherein said at least one signal via provides an electrical connection between a bond pad and a land, wherein said bond pad is electrically connected to said device electrode, and wherein said land is electrically connected to said printed circuit board.

Marked up version of once amended claim 29:

29. (Once Amended) The structure of claim 28 wherein said at least one signal via abuts said bond pad and said land.

Clean version of once amended claim 29:

29. The structure of claim 28 wherein said at least one signal via abuts said bond pad and said land.

Marked up version of once amended claim 32:

32. (Once Amended) The structure of claim 18 wherein said at least one signal via comprises copper. *colle, line 35*

Clean version of once amended claim 32:

32. The structure of claim 18 wherein said at least one signal via comprises copper.

B4
Marked up version of once amended claim 33:

33. (Once Amended) The structure of claim 18 wherein said at least one signal via comprises a thermally conductive material.

Clean version of once amended claim 33:

33. The structure of claim 18 wherein said at least one signal via comprises a thermally conductive material.

Please cancel claims 34-57.

Marked up version of once amended claim 58:

58. (Once Amended) A structure comprising:
52, 54
a substrate having a top surface and a bottom surface;

¹²
a semiconductor chip attached to said top surface of said substrate;
¹⁰
a heat spreader attached to said bottom surface of said substrate;
⁶⁶
a first plurality of separate thermally conductive vias in said substrate;
said first plurality of separate thermally conductive vias providing a connection
between said semiconductor chip and said heat spreader.

Clean version of once amended claim 58:

B5
58. A structure comprising:
a substrate having a top surface and a bottom surface;
a semiconductor chip attached to said top surface of said substrate;
a heat spreader attached to said bottom surface of said substrate;
a first plurality of separate thermally conductive vias in said substrate;
said first plurality of separate thermally conductive vias providing a connection
between said semiconductor chip and said heat spreader.

Marked up version of once amended claim 60:

60. (Once Amended) The structure of claim 59 wherein a second plurality of
⁶⁶
signal vias in said substrate provide connections between a plurality of device electrodes
¹²
of said semiconductor chip and said printed circuit board.

con 12, connection
to 22, 24

Clean version of once amended claim 60:

60. The structure of claim 59 wherein a second plurality of signal vias in said substrate provide connections between a plurality of device electrodes of said semiconductor chip and said printed circuit board.

Marked up version of once amended claim 61:

61. (Once Amended) The structure of claim 58 wherein said first plurality of separate thermally conductive vias provide an electrical connection between said semiconductor chip and said heat spreader.

Clean version of once amended claim 61:

61. The structure of claim 58 wherein said first plurality of separate thermally conductive vias provide an electrical connection between said semiconductor chip and said heat spreader.

Marked up version of once amended claim 62:

62. (Once Amended) The structure of claim 58 wherein said first plurality of separate thermally conductive vias provide a thermal connection between said semiconductor chip and said heat spreader.

Clean version of once amended claim 62:

62. The structure of claim 58 wherein said first plurality of separate thermally conductive vias provide a thermal connection between said semiconductor chip and said heat spreader.

Marked up version of once amended claim 63:

B6 63. (Once Amended) The structure of claim 60 wherein said second plurality of signal vias provide electrical connections between a plurality of bond pads and said printed circuit board, wherein each of said plurality of bond pads is electrically connected to a respective one of said plurality of device electrodes.

Clean version of once amended claim 63:

63. The structure of claim 60 wherein said second plurality of signal vias provide electrical connections between a plurality of bond pads and said printed circuit board, wherein each of said plurality of bond pads is electrically connected to a respective one of said plurality of device electrodes.

Marked up version of once amended claim 64:

64. (Once Amended) The structure of claim 60 wherein said second plurality of signal vias provide electrical connections between each one of said plurality of device

electrodes and a respective one of a plurality of lands, said plurality of lands being electrically connected to said printed circuit board.

Clean version of once amended claim 64:

64. The structure of claim 60 wherein said second plurality of signal vias provide electrical connections between each one of said plurality of device electrodes and a respective one of a plurality of lands, said plurality of lands being electrically connected to said printed circuit board.

Marked up version of once amended claim 65:

65. (Once Amended) The structure of claim 58 wherein said first plurality of separate thermally conductive vias comprise copper.

Clean version of once amended claim 65:

65. The structure of claim 58 wherein said first plurality of separate thermally conductive vias comprise copper.

Marked up version of once amended claim 66:

66. (Once Amended) The structure of claim 60 wherein said second plurality of signal vias comprise copper.

B6 [Clean version of once amended claim 66:]

66. The structure of claim 60 wherein said second plurality of signal vias comprise copper.

REMARKS

*** By the present amendment and response, independent claims 18 and 58 and dependent claims 23-24, 26-29, 32-33, and 60-66 have been amended to overcome the Examiner's objections and claims 34-57 have been canceled. Thus, claims 18-33 and 58-66 remain pending in the present application. Reconsideration and allowance of pending claims 18-33 and 58-66 in view of the following remarks are requested.

The Examiner has rejected claims 18-66 under 35 USC §102(e) as being anticipated by U.S. patent number 6,097,089 to Gaku et al. ("Gaku"). For the reasons discussed below, Applicant respectfully submits that the present invention, as defined by amended independent claims 18 and 58 is patentably distinguishable over Gaku.

The present invention, as defined by amended independent claims 18 and 58, teaches, among other things, a structure comprising a substrate having a plurality of separate thermally conductive vias that are connected to a heat spreader attached to the bottom of the substrate. As disclosed in the present application, the plurality of separate thermally conductive vias provide an effective thermal conduit to transfer heat from a chip situated on the top surface of the substrate to the heat spreader attached to the bottom of the substrate. The plurality of separate thermally conductive vias also provide an effective low resistance electrical conduit from the top surface of the substrate to the heat spreader.

Furthermore, the plurality of separate thermally conductive vias can be fabricated in a simple manner by drilling holes in the substrate and plating and filling the holes with a thermally and electrically conductive metal, such as copper. Thus, by utilizing a plurality of separate thermally conductive vias connected to a heat spreader attached to the bottom surface of a substrate, the present invention advantageously achieves a low cost, easily fabricated thermal conduit that effectively conducts heat away from a chip on the top surface of the substrate.

In contrast, Gaku does not teach, disclose, or suggest a structure comprising a substrate having a plurality of separate thermally conductive vias that are connected to a heat spreader attached to the bottom of the substrate. Gaku specifically discloses a plurality of metal protrusions having the form of a cone or frustum of a cone, which are formed on the top and bottom surfaces of metal sheet (a). See, for example, column 7, lines 46-64 and Figure 5 of Gaku. In Gaku, the plurality of metal protrusions are formed in metal sheet "a" by etching method or other similar method known in the art. See, for example, Gaku, column 6, lines 27-30. Thus, the plurality of metal protrusions disclosed in Gaku are connected together as part of metal sheet "a" and, as such, the plurality of metal protrusions are structurally different than the separate thermally conductive vias in the present invention. Also, in Gaku, the plurality of metal protrusions on the bottom surface of metal sheet "a" are not connected to a single heat spreader but are connected to individual metal pads formed in metal foil "d". See, for example, Figure 5 of Gaku.

In Gaku, resin layers “c” are situated on the top and bottom surfaces of metal sheet “a”, and metal foils “d” are situated on resin layers “c”. See, for example, column 6, lines 42-52 and Figures 1 and 5 of Gaku. The plurality of metal protrusions provide a thermal connection between a semiconductor chip mounted on a top surface of a printed circuit board and metal foil “d” on the reverse side of the printed circuit board. See, for example, column 7, lines 46-64 and Figure 5 of Gaku. Thus, the process required to achieve a thermal connection between a semiconductor chip and a metal foil in Gaku is very different than the process required to achieve a thermal connection between a chip and a heat spreader in the present invention.

Furthermore, in comparative example 1, Gaku discloses a single plated through hole that is formed in a laminate substrate to provide heat diffusion for a semiconductor chip. See, for example, column 20, lines 20-40 and Figure 10 of Gaku. However, Gaku teaches against utilizing the above single plated through hole in the laminate substrate by stating that a semiconductor package comprising the laminate substrate/through hole combination absorbs moisture and fails by partly peeling after extended testing. See, for example, Gaku, column 21, table 1. For the foregoing reasons, Applicant respectfully submits that the present invention, as defined by amended independent claims 18 and 58, is not suggested, disclosed, or taught by Gaku. As discussed above, amended independent claims 18 and 58 are patentably distinguishable over Gaku and, as such, claims 19-33 depending from amended independent claim 18 and claims 59-66 depending from independent claim 58 are, a fortiori, also patentably distinguishable over Gaku.

The Examiner has further rejected claims 58, 61, and 62 under 35 USC §101 as claiming the same invention as that of claims 1-17 of prior U.S. patent number 6,191,477 to Hassan S. Hashemi ("Hashemi"). For the reasons discussed below, Applicant respectfully submits that the present invention, as defined by amended independent claim 58, does not claim identical subject matter as Hashemi.

As stated in Chapter 800, Section 804, of the MPEP, a reliable test for double patenting under 35 USC §101 is whether a claim in the application could be literally infringed without literally infringing a corresponding claim in the patent. *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970).

The present invention, as defined by amended independent claim 58, includes the following elements: a substrate having a top and bottom surface, a semiconductor chip attached to the top surface of the substrate, a heat spreader attached to the bottom surface of the substrate, and a first plurality of separate thermally conductive vias in the substrate, where the first plurality of separate thermally conductive vias provide a connection between the semiconductor chip and the heat spreader.

In contrast, independent claims 1 and 8 of Hashemi include the following elements that are not included in amended independent claim 58: a die attach pad on the upper surface of an interconnect substrate, a second group of vias positioned about and spaced away from the die attach pad, a plurality of bond pads positioned on the upper surface of the interconnect substrate and abutting one of the vias of the second group, and a plurality of lands positioned on the lower surface of the interconnect substrate and abutting one of

the vias of the second group. Thus, since none of above elements in independent claims 1 and 8 of Hashemi is included in amended independent claim 58, amended independent claim 58 is not coextensive in scope with independent claims 1 or 8 of Hashemi. Consequently, a claim that includes only the elements of amended independent claim 58 would infringe amended independent claim 58, but would not infringe independent claims 1 or 8 of Hashemi. Thus, for the reasons discussed above, Applicant respectfully submits that amended independent claim 58 does not claim the same invention as independent claims 1 or 8 of Hashemi.

Furthermore, since the above listed elements in independent claims 1 and 8 of Hashemi are not included in amended independent claim 58, amended independent claim 58 is not an obvious variation of independent claims 1 or 8 of Hashemi.

Dependent claims 61 and 62 add a limitation to amended independent claim 58 requiring the first plurality of vias to provide an electrical connection and a thermal connection between the semiconductor chip and the heat spreader. However, for reasons similar to those stated for amended independent claim 58, even with the addition of the above limitations, claims 61 and 62 do not claim the same invention as independent claims 1 or 8 of Hashemi. Thus, Applicant respectfully submits that amended independent claim 58 and dependent claims 61 and 62 are not subject to a double patenting rejection.

The Examiner has further rejected claims 18-57, 60, and 63-66 under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims

1-17 of Hashemi. For the reasons discussed below, Applicant respectfully submits that amended independent claim 18 is not an obvious variation of independent claims 1 or 8 of Hashemi.

The present invention, as defined by amended independent claim 18, includes the following elements: a substrate having a top surface for receiving a chip, a printed circuit board attached to the bottom of the substrate, at least one signal via in the substrate providing an electrical connection between a device electrode of the chip and the printed circuit board, and a plurality of separate thermally conductive vias in the substrate, where the plurality of separate thermally conductive vias are coupled to a heat spreader attached to the bottom surface of the substrate.

In contrast, independent claims 1 and 8 of Hashemi include the following elements that are not included in amended independent claim 18: a die attach pad on the upper surface of an interconnect substrate, a second group of vias positioned about and spaced away from the die attach pad, a plurality of bond pads positioned on the upper surface of the interconnect substrate and abutting one of the vias of the second group, and a plurality of lands positioned on the lower surface of the interconnect substrate and abutting one of the vias of the second group. Thus, since none of the above elements in independent claims 1 and 8 of Hashemi is included in amended independent claim 18, amended independent claim 18 cannot be an obvious variation of independent claims 1 or 8 of Hashemi. Thus, as discussed above, amended independent claim 18 is not obvious variations of independent claims 1 or 8 of Hashemi. Moreover, for reasons similar to

those stated above, claims 19-33 depending from amended independent claim 18 and claims 58-66 are also not obvious variations of independent claims 1 or 8 of Hashemi. Thus, Applicant respectfully submits that pending claims 18-33 and claim 58-66 are not subject to a double patenting rejection.

Based on the foregoing reasons, claims 18-33 and 58-66 pending in the present application are in condition for allowance and an early allowance of pending claims 18-33 and 58-66 is respectfully requested.

Respectfully Submitted,
FARJAMI & FARJAMI LLP

Date: 6/13/02



Michael Farjami, Esq.
Reg. No. 38, 135

Michael Farjami, Esq.
FARJAMI & FARJAMI LLP
16148 Sand Canyon
Irvine, California 92618
Telephone: (949) 784-4600
Facsimile: (949) 784-4601

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed: Commissioner of Patents and Trademarks; Washington, D.C. 20231

Date of Deposit: 6/13/02

Ali Shalchi
Name of Person Mailing Paper and/or Fee

Ali Shalchi 6/13/02
Signature Date